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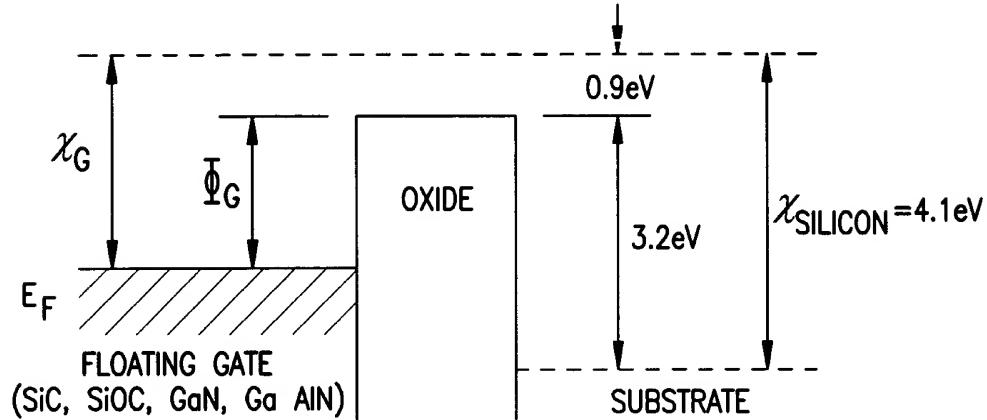


FIG. 1A
(PRIOR ART)

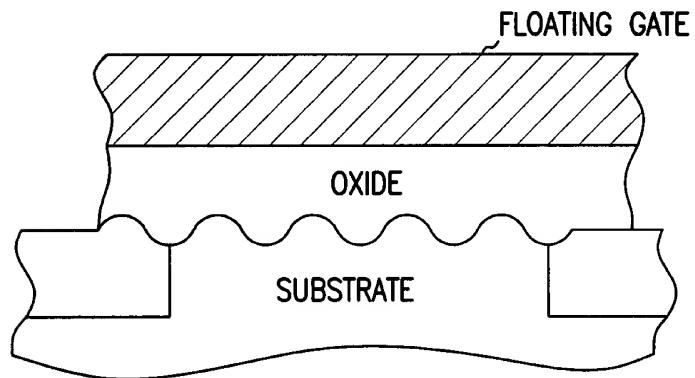


FIG. 1B
(PRIOR ART)



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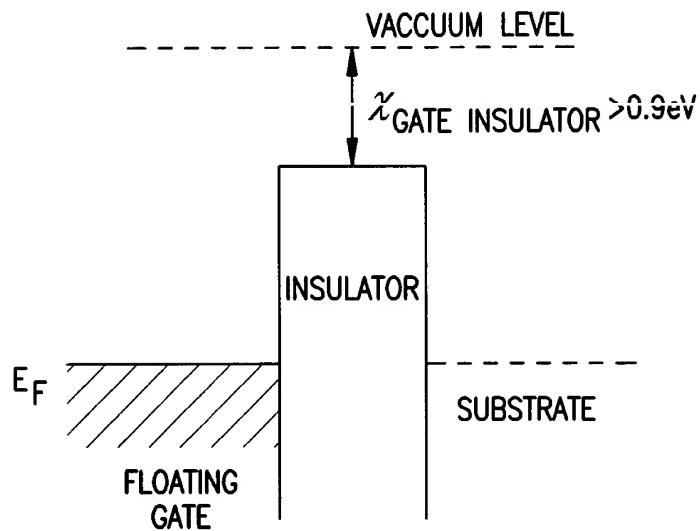


FIG. 1C
(PRIOR ART)

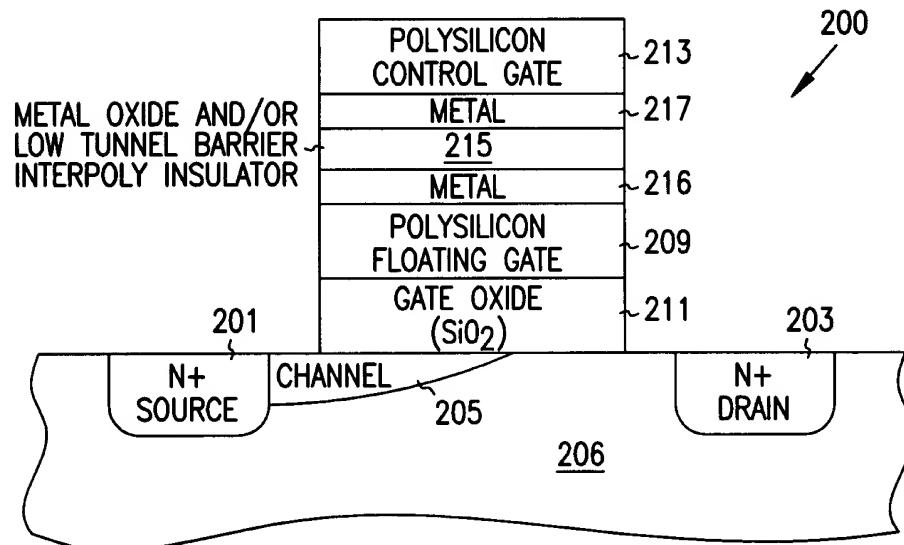


FIG. 2



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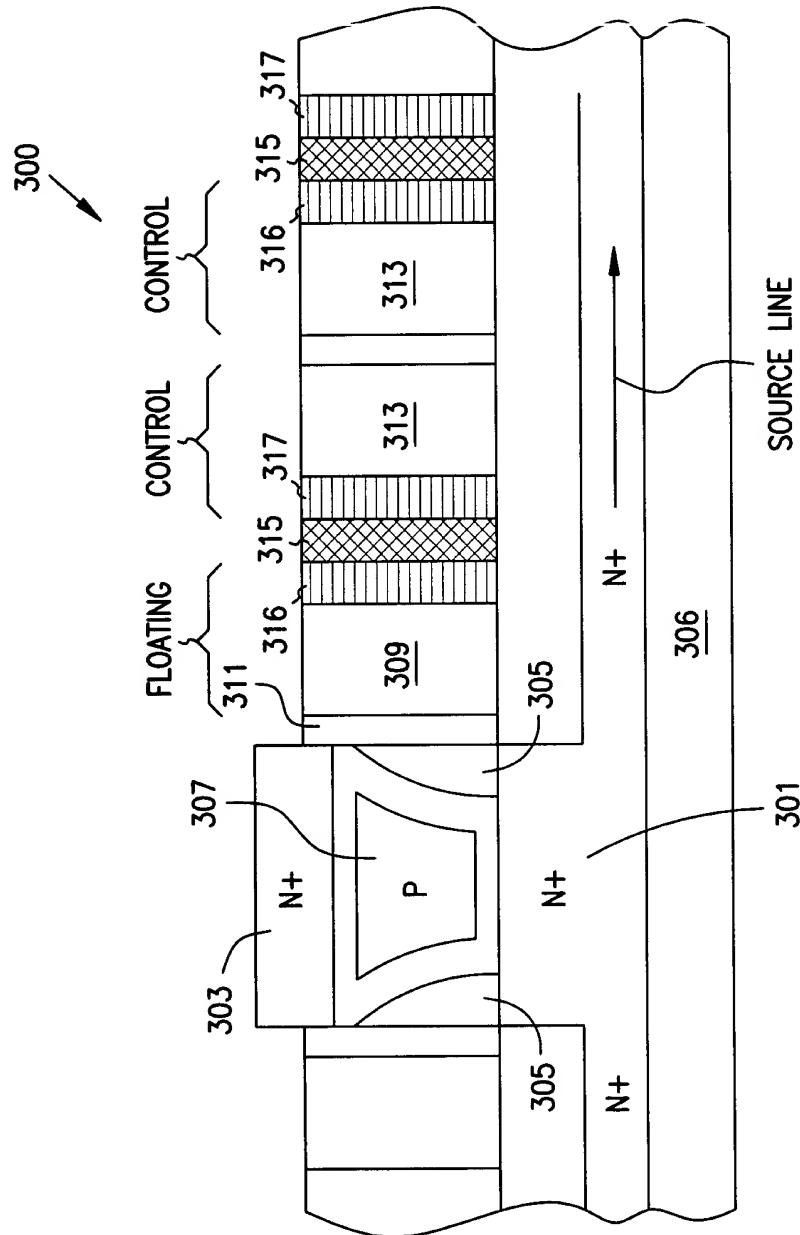


FIG. 3



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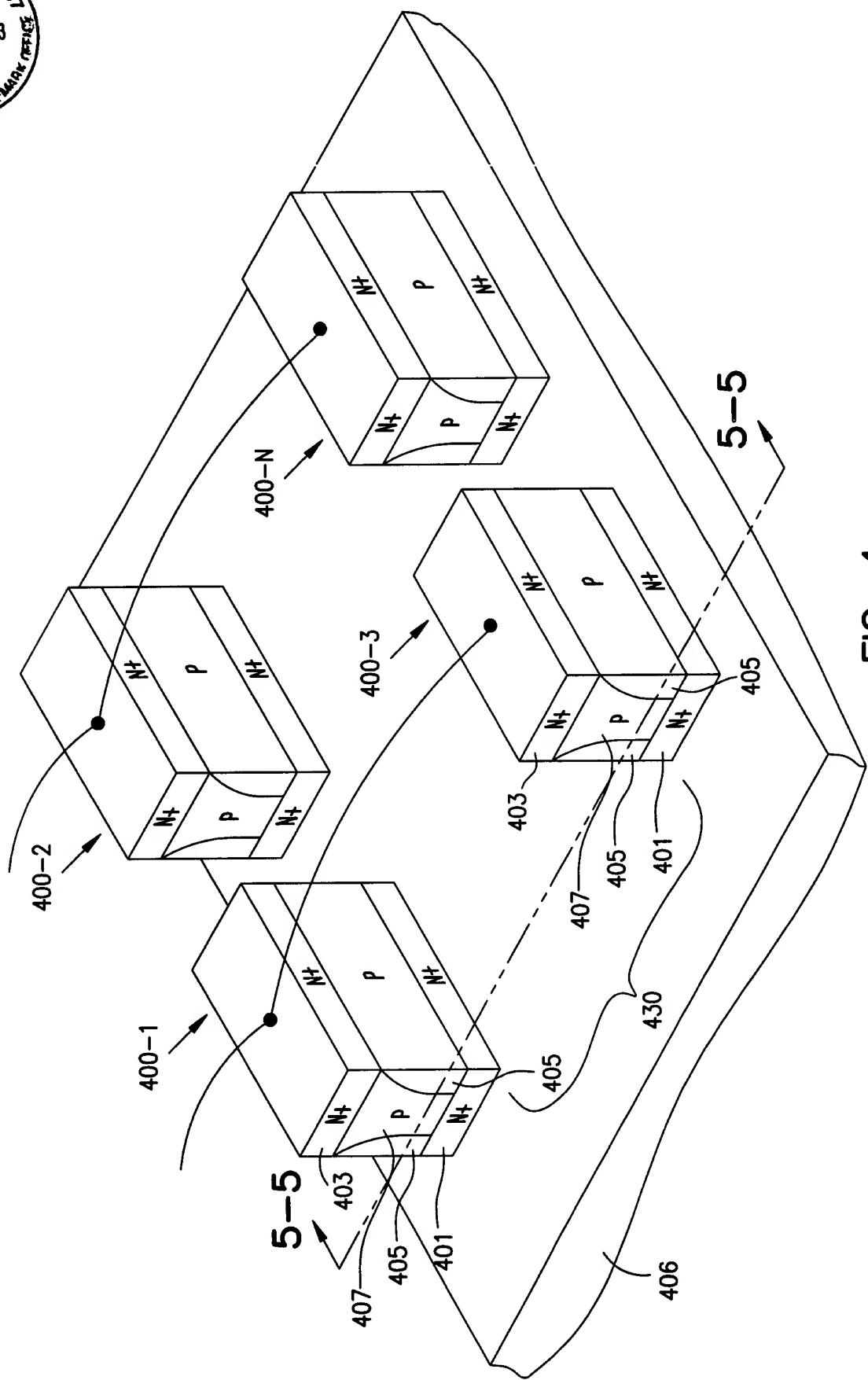


FIG. 4



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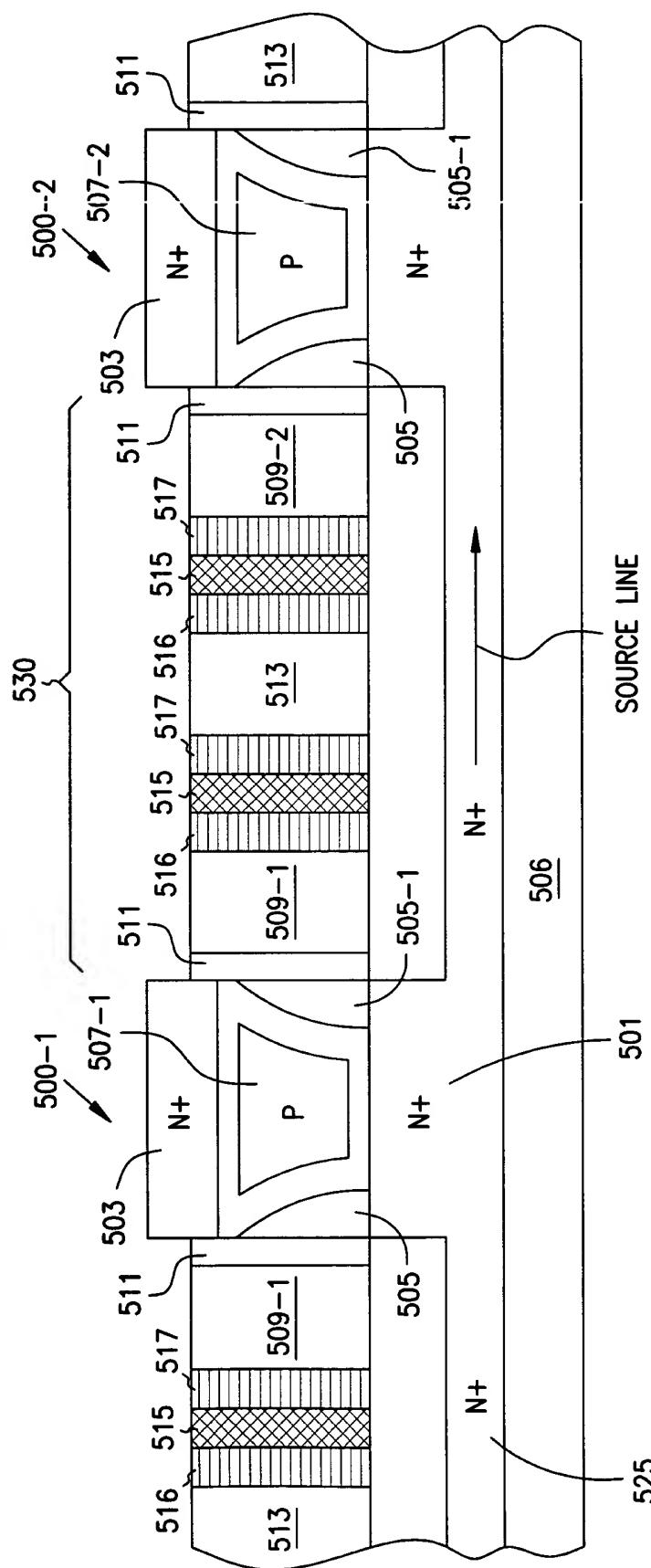


FIG. 5A



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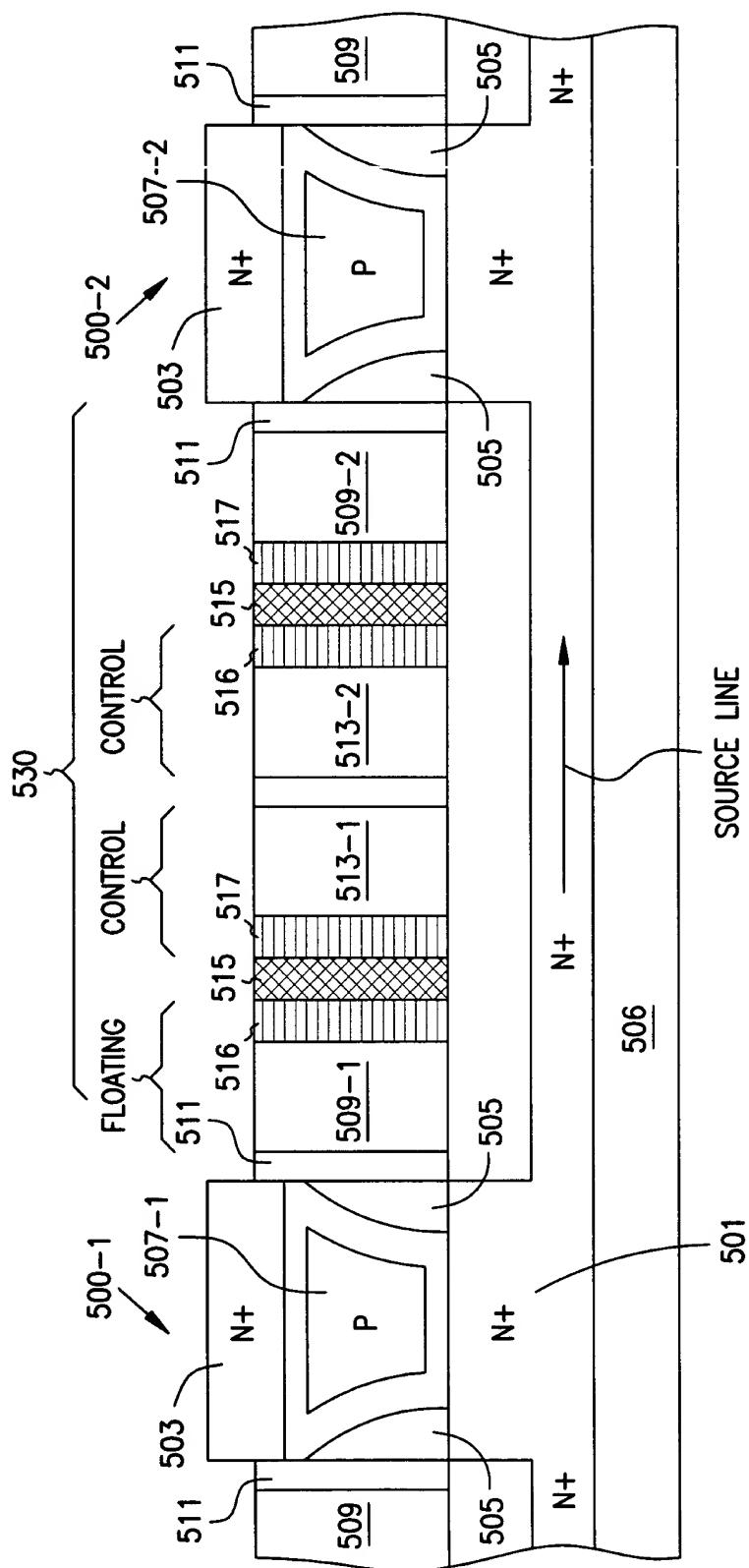


FIG. 5B



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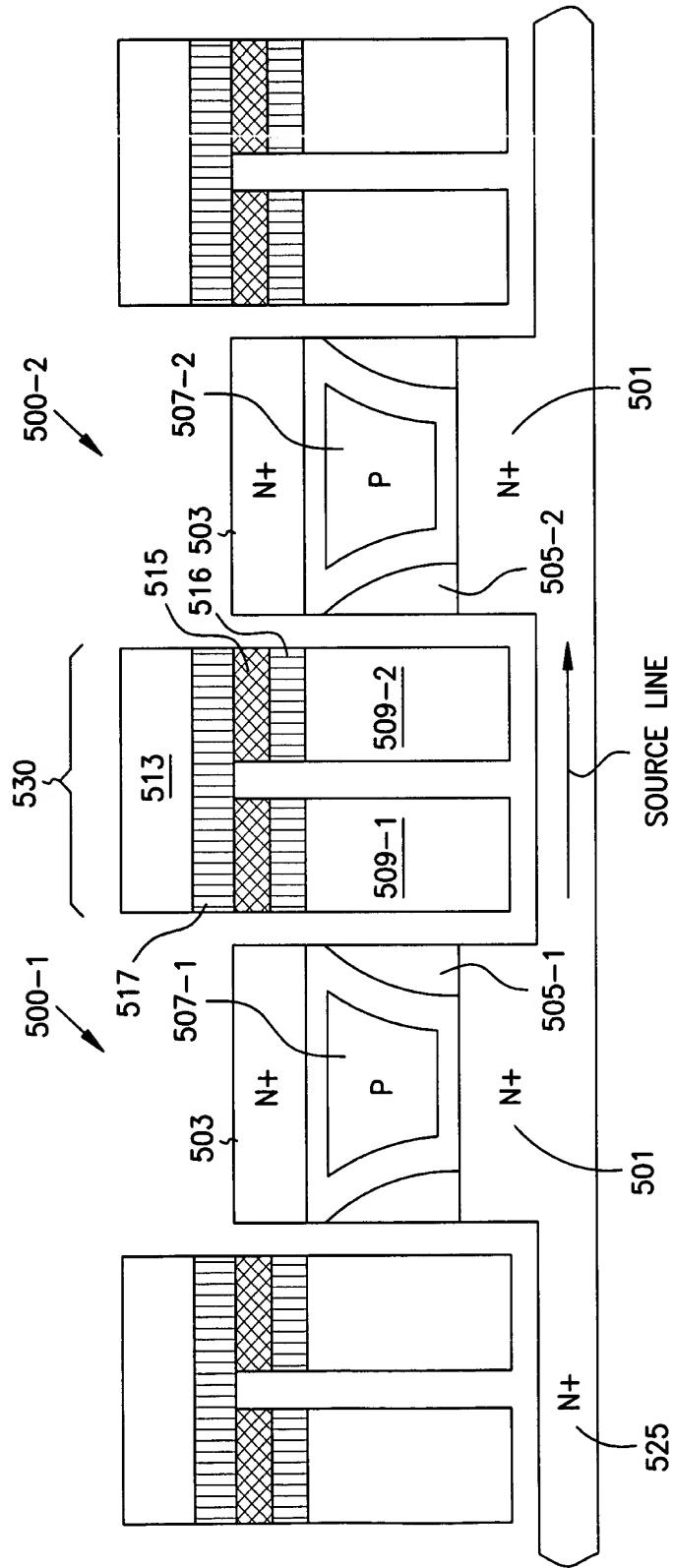


FIG. 5C



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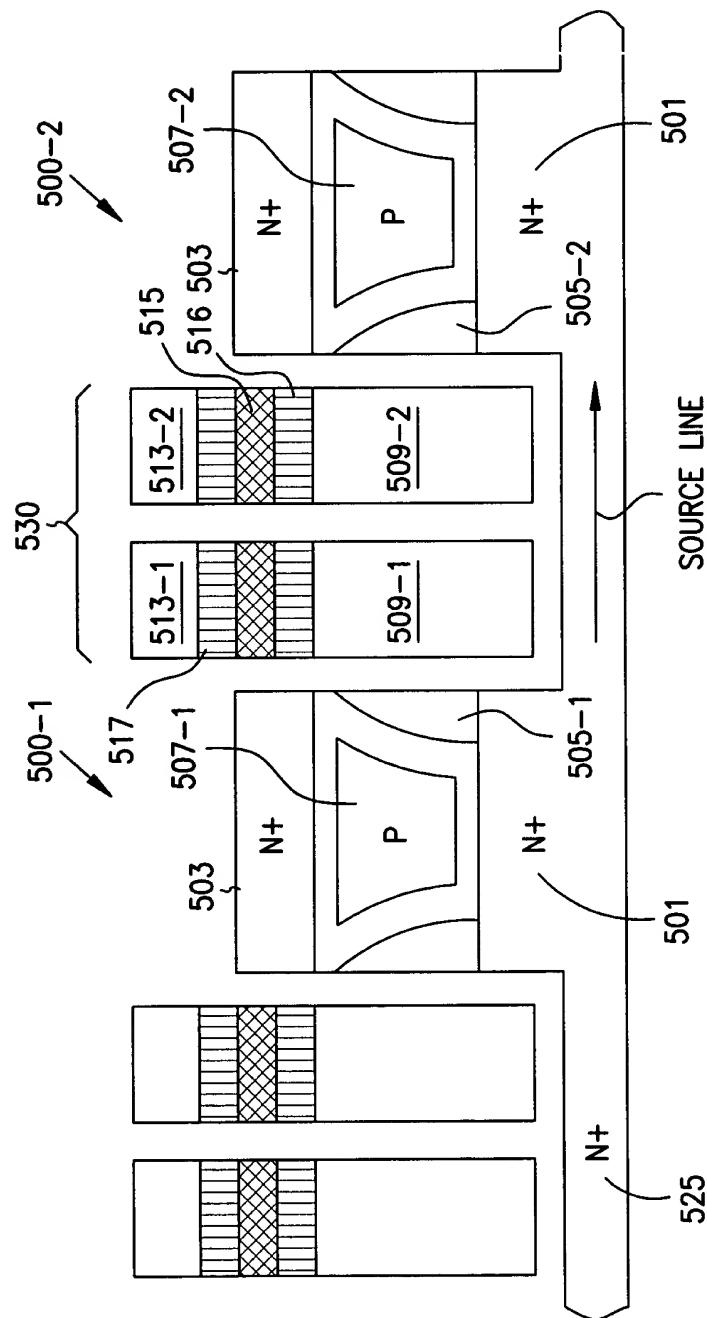


FIG. 5D



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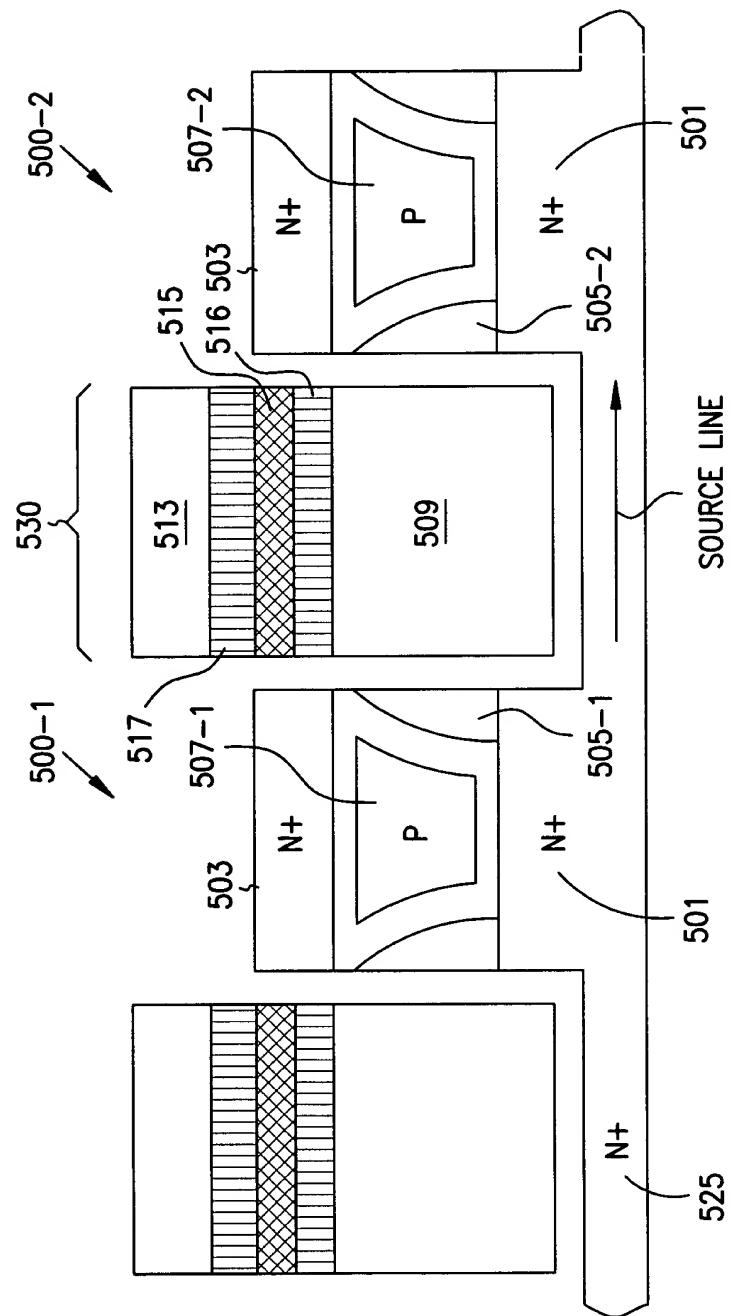


FIG. 5E



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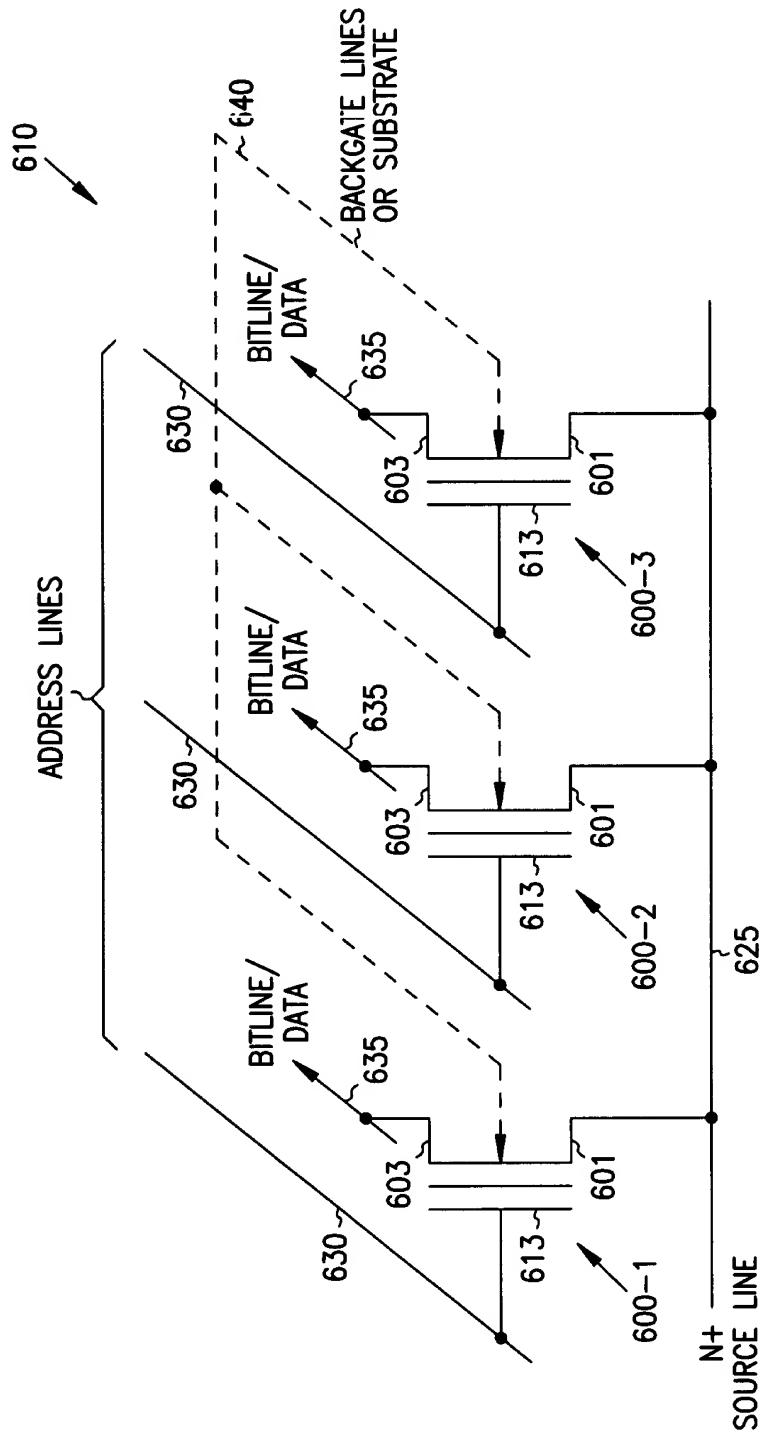


FIG. 6A



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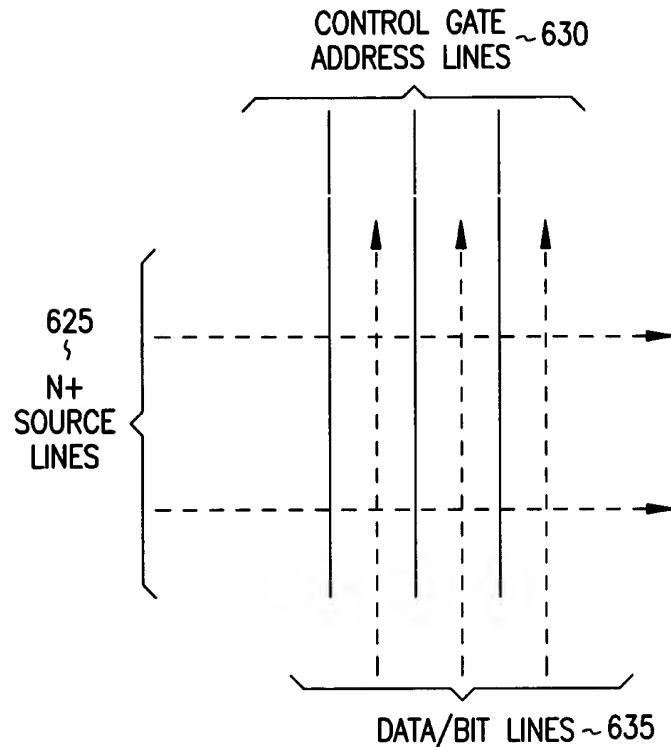


FIG. 6B

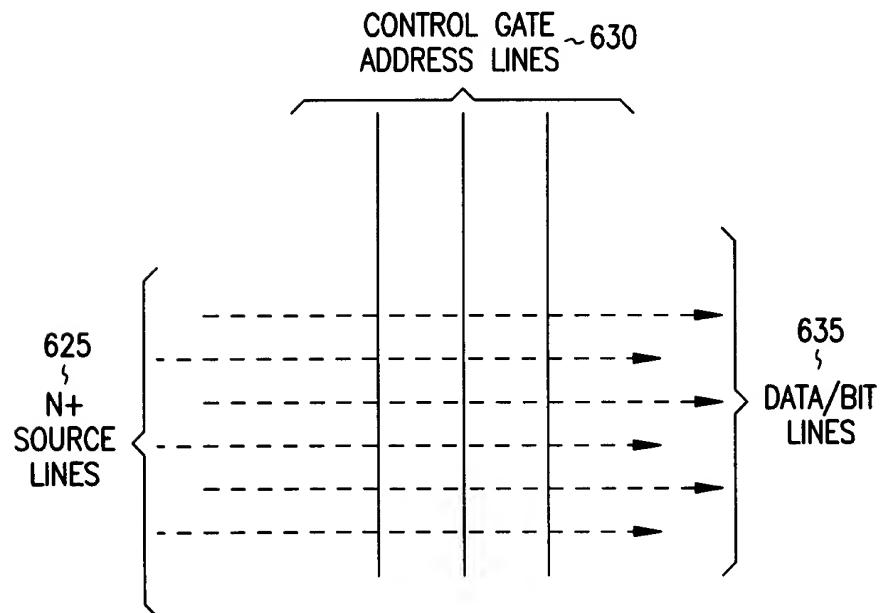


FIG. 6C



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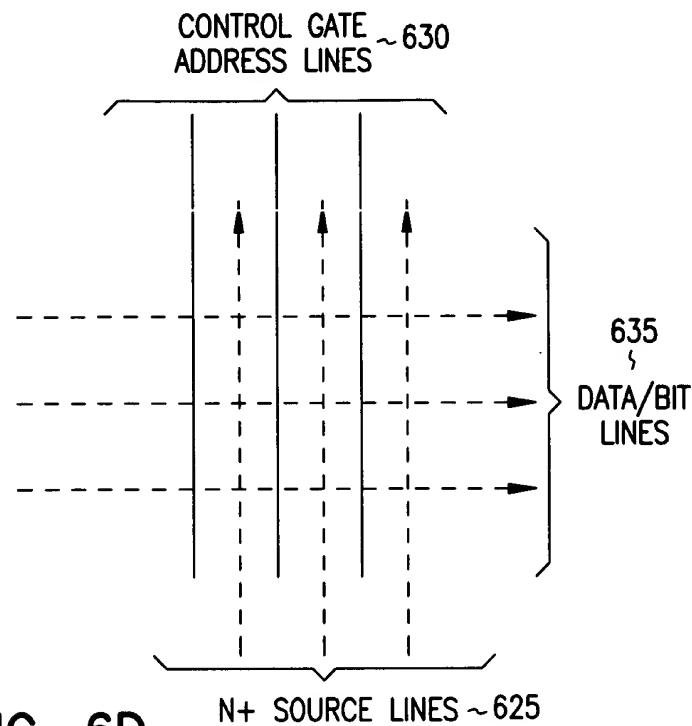


FIG. 6D

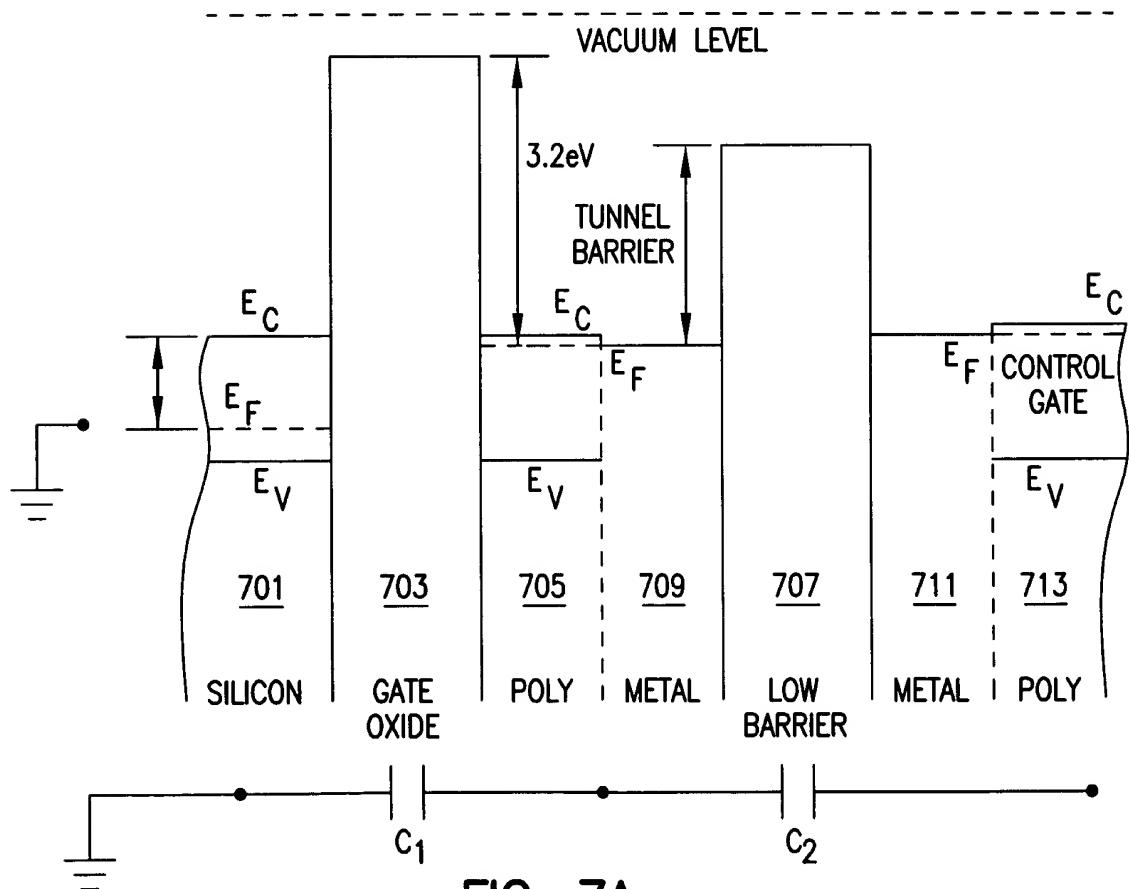


FIG. 7A



TITLE: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
 INVENTORS NAME: Leonard Forbes
 DOCKET NO.: 1303.027US1

REPLACEMENT SHEET

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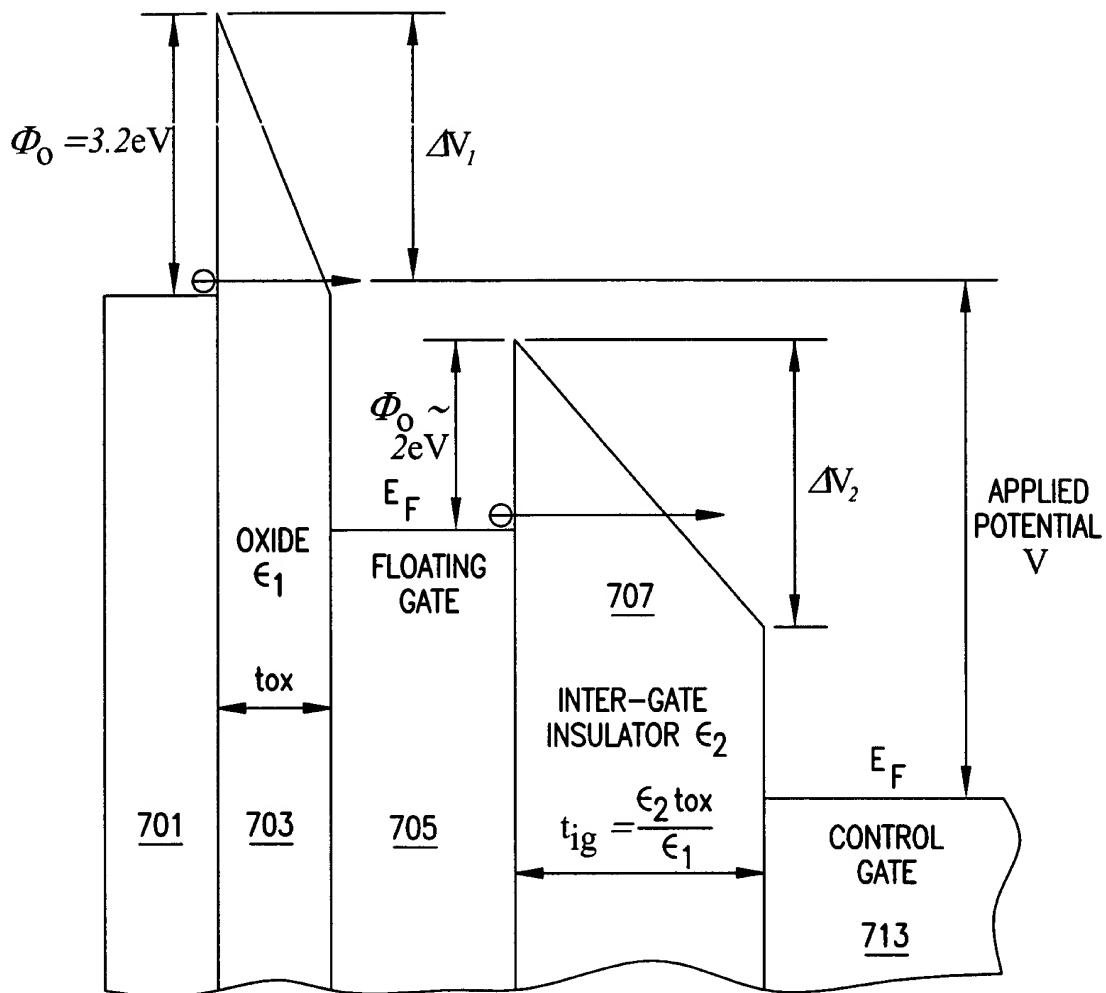
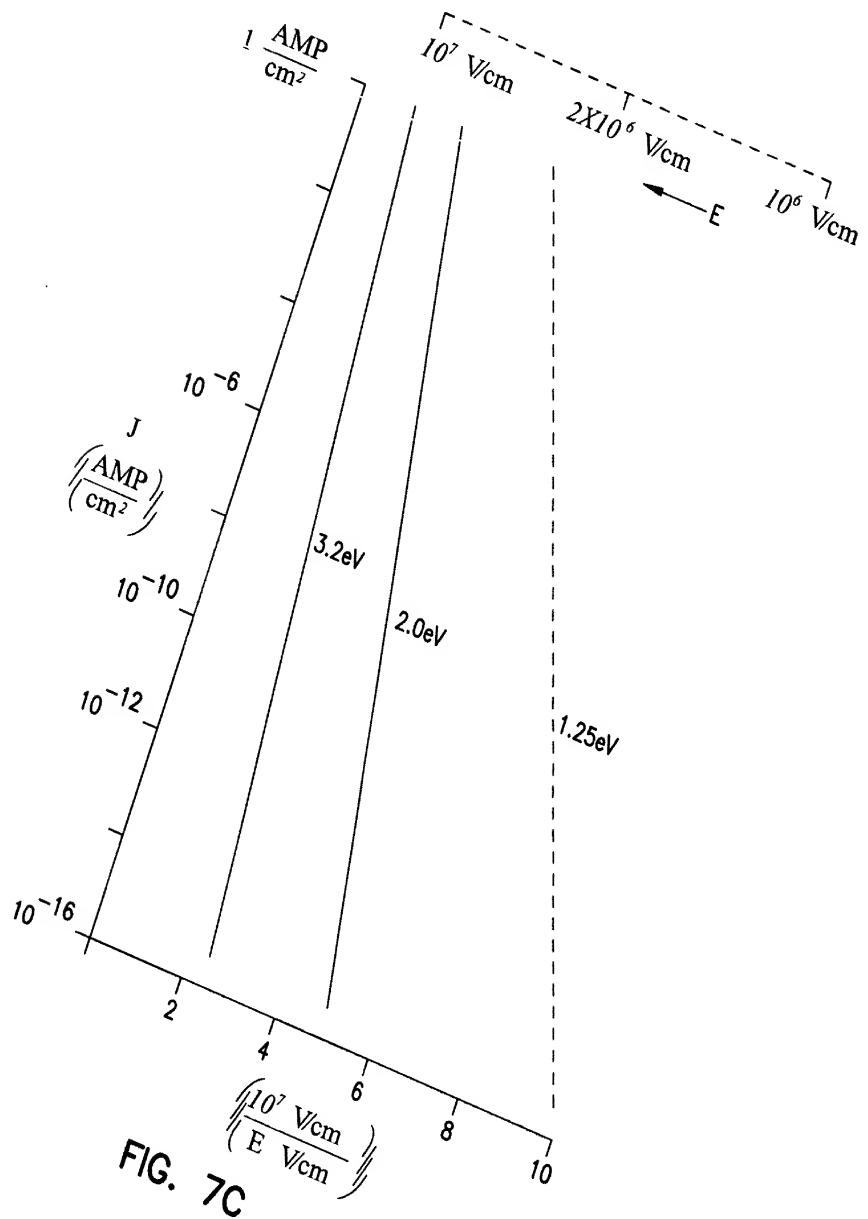


FIG. 7B



TITLE: IN-SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
 INVENTORS NAME: Leonard Forbes
 DOCKET NO.: 1303.027US1
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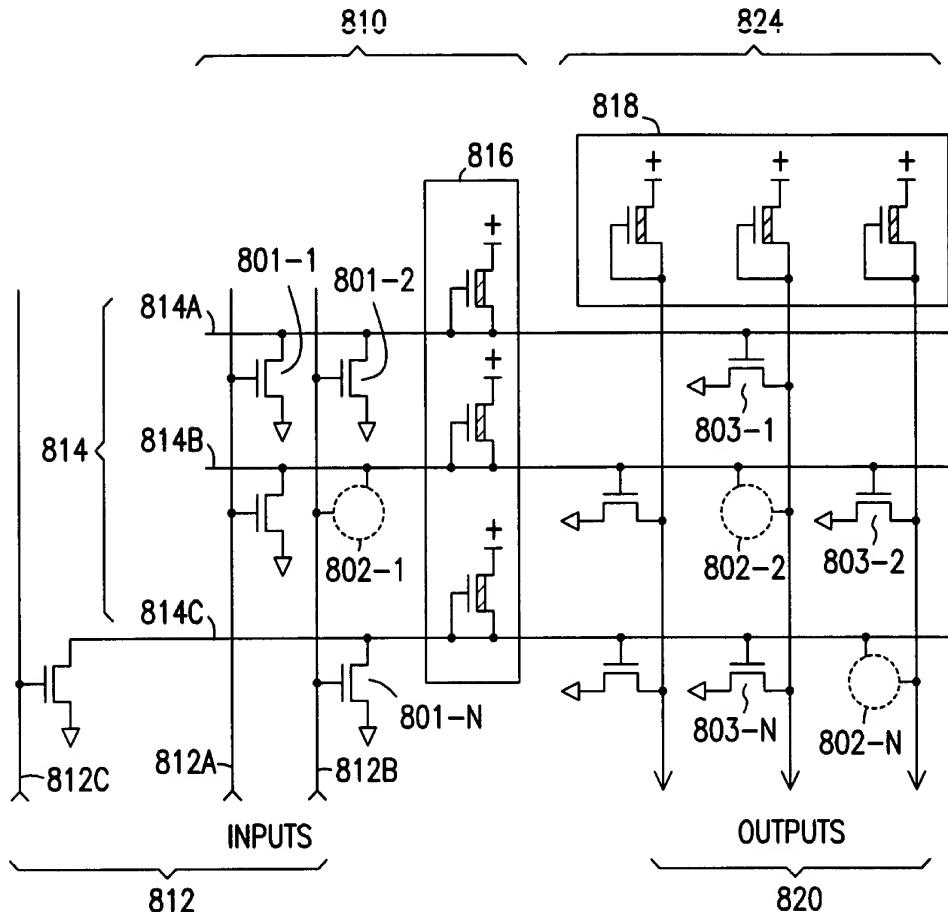


FIG. 8



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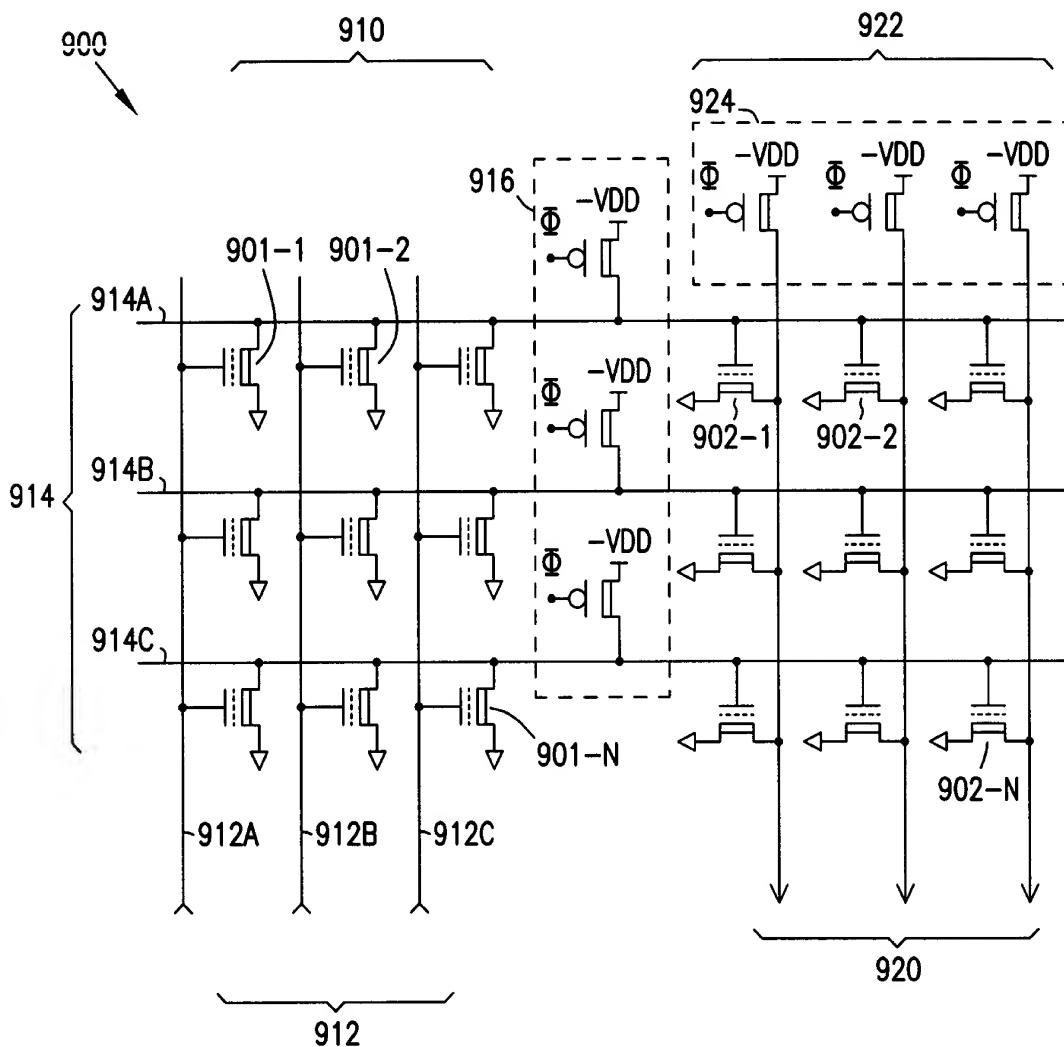


FIG. 9



TITLE: IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
INVENTORS NAME: Leonard Forbes
DOCKET NO.: 1303.027US1

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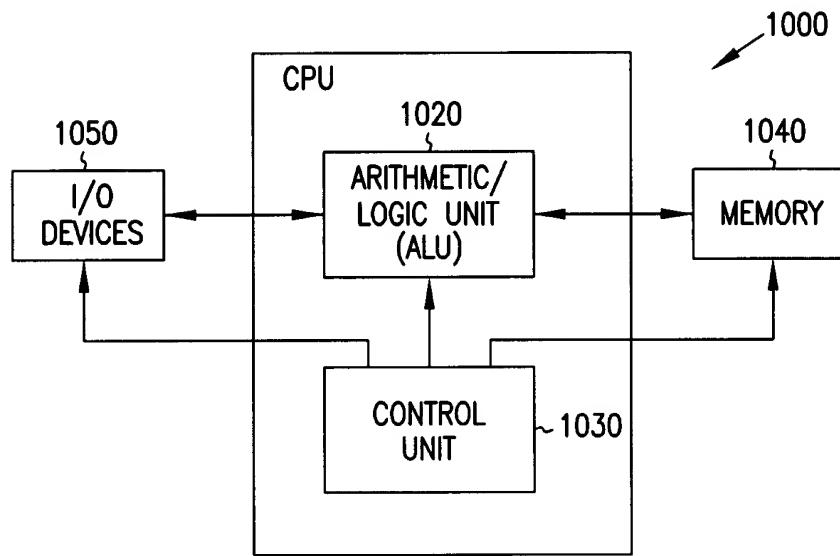


FIG. 10